A New Approach to Evaluating PCIe® Link Health

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WHITE PAPER

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Introduction

The trend toward ever faster data rates is matched with a corresponding trend: an ever-increasing amount of time is needed to validate new technologies. As a result, development bottlenecks are impacting product time-to-market cycles as engineering teams struggle to keep up with increasing test times when using legacy test and measurement solutions.

Not only are the testing times and complexities increasing, but consumers continue to hold high expectations for product performance and interoperability. End users of PCIe-compatible devices expect to plug any PCI Special Interest Group (PCI-SIG®) compliant add-in card (AIC) into any PCI-SIG compliant system board of the same generation or older. This expectation means that testing must be stringent, and that each vendor must have adequate design margins to ensure interoperability with all other PCI-SIG compliant products.

When two products do not work together consumers face the problem of who to blame. Is it the system board manufacturer? The add-in-card manufacturer? Both? Who does the consumer go to when there is a problem? Unfortunately, issues like this can cause both vendors to undergo cost-intensive investigations into who is at fault, and these investigations can take months, and cost upwards of millions of dollars to fully resolve.

While slim design margins are not the *only* way in which two boards may struggle to interoperate with one another, having adequate design margins significantly reduces the risk of not being interoperable with other PCI-SIG compliant products. This can save vendors both time and money in reducing the number of situations where they need to resolve interoperability issues.

Margin Testing Today

Until very recently, there were just two common methods to test for design margins in HSIO designs, and both came with associated pros and cons.

1. **Scope/BERT** – test systems consisting of an oscilloscope, Bit Error Rate Tester (BERT), and Sigtest software available from the PCI-SIG. This solution can cost a half million dollars or more.

2. On-chip Lane Margining (**LM**) – tools offered by silicon manufacturers to board manufacturers. This option is free starting with the PCIe Gen 4 standard.

The most comprehensive testing toolset today remains the Scope/BERT. This solution can complete all validation and compliance testing needed to satisfy the standard and certify compliance of PCIe devices, but it comes with high levels of complexity, and a price tag that smaller manufacturers often cannot justify or afford. At a cost of a half-million dollars or more per system, even larger vendors have a limited number of systems to perform their testing.

Even experienced engineers may need several days to get these test systems fully operational, and full testing of 16-lane links can take weeks beyond initial setup if issues arise. These test systems are superior to any on-chip LM tools available from silicon manufacturers, but they are expensive, time consuming, and often require high levels of expertise to operate properly. This equipment is required for full compliance and extensive silicon validation, whereas the LM tools can be used for limited-scope checks without the overhead.

While free LM tools provide some performance insight at no cost and are less complex than Scope/BERT systems, they have numerous limitations. First, LM tools are only capable of lane margining at their own receivers. The user is capable of only investigating margins of the DUT receiver path (Rx), but unable to margin the DUT transmitter (Tx) path.

Another drawback of LM tools is they vary from vendor to vendor, requiring a learning curve for engineers to familiarize themselves with each tool. This repeated ramp-up could be overcome with a consistent third-party method. Finally, the inherent unit-to-unit variability that is inextricably linked to chip variability will exist. This often requires multiple testing cycles to increase the measurement population and rely on measures of central tendency.

Notably, the testing methodologies between these methods differ. The Scope Tx approach (**Figure 2**) uses real-time sampling to construct eye diagrams, where on-chip LM tools rely on sweeping the Rx sample location until errors are observed (to determine eye width). Some LM implementations also determine eye height with vertical sampler adjustments (**Figure 1**). Real-time signaling is the better option as engineers see an independently constructed eye diagram. The LM approach is a trade-off with a loss of accuracy and consistency when cost and complexity of the Scope/BERT cannot be justified.

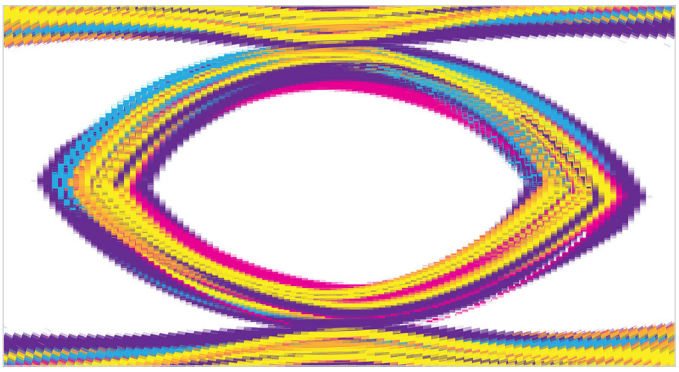

Figure 1: Example On-Chip Receiver Eye Diagram

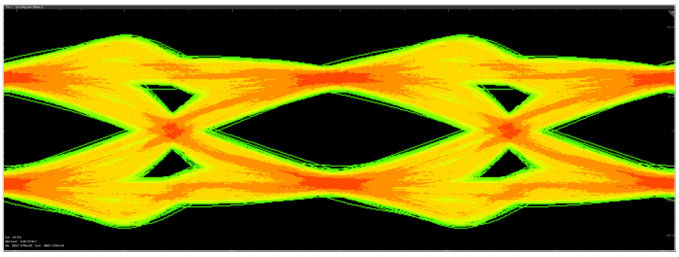

Figure 2: Real Time Analog Eye Diagram

Bringing consistency between true link operation and the test environment is key, with two key considerations being the type of traffic (signal pattern) and the type of receiver used. Scope/BERT systems use a model receiver with repetitive signal patterns to stress and test the transceivers as outlined in the PCIe standards. On-chip LM tools use a physical receiver with real traffic on the link. The nature of these tests causes the discrepancy. The Scope/BERT systems are not built with a PCI Express receiver and have memory/storage and signal post processing limitations. The LM tools rely on a physical receiver implementation acting as a link partner with true traffic flow instead of artificial signal patterns.

Both methods have pros and cons. Importantly, only the Scope/BERT methodology solution allows for full validation and compliance testing. LM tools are not capable of addressing all required tests to ensure validation and compliance to the PCIe standard.

Pros and cons for existing testing methods

Scope/BERT System (Oscilloscope + BERT + SigTest software)	
Advantages: • Provides a comprehensive suite of tests suitable for full validation and compliance testing • Test specifications are written with the scope as the reference • Capable of constructing full channel Tx eye diagram, jitter decomposition, and receiver stressed eye calibration • Uses real-time sampling to construct eye diagrams • General purpose test equipment limited to testing one technology	**Disadvantages:** • Cost-prohibitive • Test times can be days to weeks depending on testing requirements • Testing complexities level often requires senior-level engineering expertise • Complexities of the system can lead to errors and incorrect conclusions • Artificial signal patterns don't properly capture multiple crosstalk impacts from real aggressors

On-Die Lane Margining Tool	
Advantages: • Standardized tool starting with the PCI Express 4.0 standard • Provided free to designers from silicon vendors • Developed specifically for identifying margins at the vendor's receivers • Easy to use if familiar with PCIe • Rx margin data available in minutes, not days or weeks	**Disadvantages:** • Do not use real-time analog signals • Are not often offered on devices below 16 GT/s • Cannot be used for complete validation or compliance testing • Introduces unit to unit variability • Difficult to vary design or test parameters in a significant way • Software interface non-standardized

A New Margin Testing Alternative

Until now, when design teams needed to evaluate PCIe link health they've had to live with the gap that exists between LM tools and Scope/BERT systems and simply accept the disadvantages outlined above.

Into this gap, Tektronix has introduced a new tool: the TMT4 Margin Tester. Designed for engineers who are testing PCIe Gen 3 and Gen 4 devices today, the TMT4 Margin Tester, offers:

- Evaluation of link health with Tx and Rx testing in minutes, not days
- Out-of-the-box ease of use, even by junior engineers or technicians with little-to-no PCIe experience
- A much more widely affordable link health evaluation tool

Fast Link Health Evaluation

The TMT4 Margin Tester requires less than 10 minutes to set up and can provide a high-level link-health evaluation of a Gen 3 or Gen 4 device in as little as two minutes. In that short amount of time users can generate eye diagrams, for each lane and preset combination, which represent the error-free region of the link formed between the DUT and the Margin Tester. The speed with which they are produced offers the potential for dramatically faster insight into DUT link health.

Moreover, the Margin Tester shows the performance of the link not only by displaying eye diagrams, but also by displaying how the Margin Tester's receivers were adjusted to maximize the generated eye. Having both pieces of information is critical to understanding performance, as some eyes may need especially high levels of equalization to form the link.

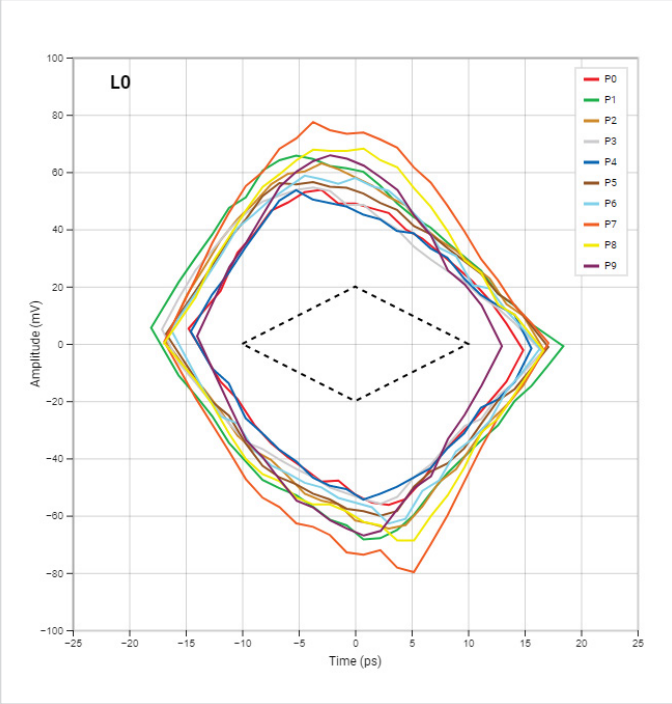

Figure 3. Eye Diagrams Are Presented to the User by the TMT4 Margin Tester in Real Time.

The speed of the TMT4 Margin Tester means that teams can now conduct regular, even frequent, performance checks of the link and quickly identify gross errors for any lane and preset combination. If, for example, an engineer wants to quickly see the effects of a BIOS change on the health of the link, they can scan the DUT, update the BIOS, scan the DUT again, and in minutes be able to evaluate the effect those changes had on the link performance.

Greater Ease of Use

Because the TMT4 Margin Tester supports most common PCIe form factors like CEM, M.2, U.2, and U.3, it can link with the majority of the PCIe devices available today. That enables the testing of a wide range of possible DUTs and evaluation of most common PC components, such as motherboards, graphics cards and SSDs.

Margin Tester users quickly gain the experience they need to get results as there are just two scan options, Quick Scan, and Custom Scan available. Both include DUT Tx and DUT Rx tests, and can be run from the same physical setup, with the only difference being the level of control given to the user.

The fastest option, Quick Scan enables frequent evaluation of link health and is of great use for a fast view of natural link training between a DUT and TMT4. Custom scans, on the other hand, enable users to force specific test parameters in order to do a more thorough evaluation of their Tx signal paths. It is most useful when a deeper investigation into specific lane-preset combinations is needed, or a more comprehensive test of all lanes and presets is desired.

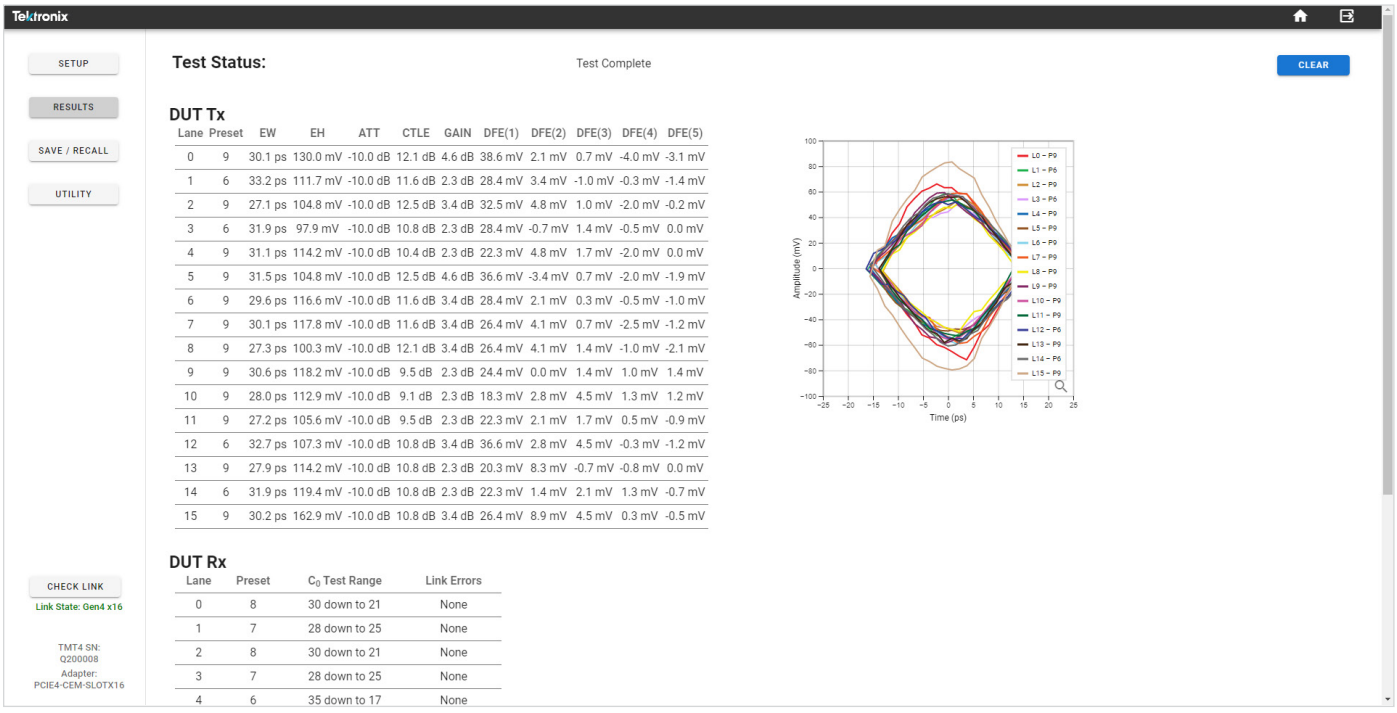

Figure 4. Quick Scan Results Table with Link Training Parameters (top left), Eye Diagrams (top right), and Rx Test (bottom).

A Margin Test Tool for Everyone

The tradeoffs between LM tools and Scope/BERT systems have exacerbated the two trends noted at the outset of this white paper, namely 1) the struggle to validate PCIe compatible devices without adding more time to compressed development cycles and 2) the potential for an ever-greater number of situations where vendors need to resolve interoperability issues.

Without seeking to replace either LM tools or Scope/BERT systems, the TMT4 Margin Tester provides the industry with a much-needed complementary tool. With a focus on reducing test times, improving ease of use, and offering a cost-effective solution to the PCIe testing market, it's a tool that more vendors can afford to invest in. Design teams will gain faster insight into the link health of their DUTs with tests that evaluate the Tx and Rx signal paths of a live link in minutes. The value propositions of the TMT4 have significant implications on overall design workflows by leveraging its speed and ease of use to help minimize testing bottlenecks and allowing for more frequent link health evaluation during development.

The TMT4 Margin Tester is one of many test solutions offered by Tektronix for PCI Express. Learn more about the full suite of these solutions online.

About the Author

Michael Seaholm is a Product Manager for Performance Oscilloscopes at Tektronix, Inc. He has spent 4 years as a Product Manager in the Test and Measurement industry, including 3 years at Fluke Corporation in their Electrical Calibration Business and over a year at Tektronix. Michael has a BSEE in Electrical Engineering from Montana State University and has spent his career in Product Management focused on bringing new innovations to test and measurement through consistent engagement with customers.

Figure 5. TMT4 Margin Tester (center), CEM Edge Adapter (right) and Networked Access to Results on PC (left).

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